REMARKS

This amendment and response is in response to the Office Action dated May 19, 2006. Claims 1-23 will be pending after entering the attached amendment. Claims 21-23 are new. No new matter has been added.

Claims 6, 12 and 18 have been objected to as being in improper dependent form for allegedly failing to further limit the subject matter of the previous claim.

Claims 1 and 7 have been rejected under 35 U.S.C. §102(e) as being anticipated by previously cited U.S. Patent No. 674,065 to Suh. Claims 1-4, 6-10, 12-16 and 18-20 have been rejected under 35 U.S.C. §103(a) as being patentable over the combination of U.S. Publication No. 6,070,218 to Giles et al and Suh. Claims 5, 11 and 17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Giles, Suh and further in view of Monahan, U.S. Publication No. 4,001,783.

With regard to the objection of claims 6, 12 and 18, Applicants respectfully traverse. Claim 6 refers to "defining the control bit values according to system requirements" wherein the system comprises a processor, at least one interrupt source, and at least one interrupt input. Claims 12 and 18 recite corresponding structure. The dependent claims further limit the parent claims by how the control bit values are defined. Therefore, Applicants respectfully request the withdrawal of the objection to the claims.

In making the 35 U.S.C. §102(e) rejection of claims 1 and 7 on page 3 of the Office Action, Figure 3 ("mapping is0...is25 to INT1 or INT2") is referred to as disclosing the feature of mapping each of the plurality of interrupt sources to each of

the plurality of interrupt inputs. However, each of the plurality of interrupt sourcesis not mapped to each of the INT1 or INT2 signal of Figure 3.

A careful reading of the specification reveals that the INT1 or INT2 signals of Suh are merely an indication of an interrupt condition depending upon the interrupt mode. Suh discloses, "The CPU 1 senses an interrupt in response to the interrupt signal INT1 or INT2." (see column 6, lines 33-34). This is not disclosure of or a suggestion that an individual interrupt source is mapped to either INT1 or INT2.

Rather, the finally selected interrupt sources correspond to either the Vector_I or Vector_F, where either the Vector_I or Vector_F is generated through the vector generator 70 (see column 6, lines 24-28). The Vector_I or Vector_F is used to identify the corresponding branch instruction.

Elements 40 and 50 of Figure 3 in the Suh patent perform the function of determining priority between enabled interrupt sources, the two circuits do not perform the functions as recited in claims 1 and 7.

Finally, Claims 1 and 7 have also been rejected under 35 U.S.C. §103(a) as being patentable over the combination of U.S. Publication No. 6,070,218 to Giles et al and Suh. In making the rejection under 35 U.S.C. §103(a), the Office Action substitutes the Giles patent as disclosing the feature of mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs as recited in independent claim 1, and similarly in independent claim 7. By doing so, the Office appears to be conceding that the Suh patent does not disclose or suggest the same feature that it is alleged to teach in the rejection under 35 U.S.C. §102.

Based on the above, Applicants respectfully submit that the Suh patent does not disclose or suggest mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs as recited in independent claim 1, and similarly in independent claim 7.

Claims 1-4, 6-10, 12-16 and 18-20 have been rejected under 35 U.S.C. §103(a) as being patentable over the combination of U.S. Publication No. 6,070,218 to Giles et al. and Suh. The Giles patent is directed to a system that holds a interrupt signal to ensure that such a signal is asserted long enough for the processor to receive and respond to it. The Giles patent attempt to accomplish this task by routing hardware interrupts to a capture and hold mechanism.

As stated in the rejections of claims 1 and 7, the Giles patent does not disclose or suggest a plurality of interrupt inputs. Applicants agree the Giles patent does not disclose or suggest mapping the plurality of interrupt sources to each of the plurality of interrupt inputs, and submit that the Suh patent, based on the above, does not overcome this deficiency.

At best the Giles patents discloses a circuit used for a different purpose and application. The interrupt circuits cited in the rejection and shown in Figures 4 and 5 of the Giles patent include an INTERRUPT signal. In the circuit described in Figure 4, the INTERRUPT signal allows for a global interrupt signal to be asserted. If the INTERRUPT signal is in a non-enabling state it prevents all interrupt requests from being enabled to the interrupt input. (See column 5, lines 49-59).

The same can be said for the INTERRUPT signal described in Figure 5 of the Giles patent. (see column 5, line 65-column 6, line 2, and column 6, lines 16-20) as it is applied to AND gates 604 and 618.

In addition, the interrupt circuit of Figure 5 includes interrupt acceptance circuit 606 to provide an enforcement of the condition that an interrupt which begins to trigger an exception be held long enough to enforce the complete transfer of control to the exception handling routine (see column 6, lines 50-55). The interrupt acceptance circuit 606 receives the output from logic element 604 and based on the outputs of logic elements 616, 614, and 612 will further allow an interrupt signal to be output from global interrupt determination unit 608.

This is different than Applicants' claimed system and method. The Suh patent does not overcome these deficiencies.

As for the motivation to combine the teachings of the Suh patent with those of the Giles patent, it is unclear if one of skill in the art would have resolved the increased system performance teachings of the Suh patent with the teachings of holding an interrupt signal to ensure that the complete transfer of control to the exception handling routine (see column 6, lines 50-55 of the Giles patent) would be accomplished.

In making the rejection of independent claim 14, the Office admits that the Giles patent does not teach plural interrupt inputs (see page 7 of the Office Action), and relies on the Suh patent to disclose such a feature. However, the Suh patent as explained above does not disclose plural interrupt inputs.

Even assuming, *aguendo*, that the Suh patent does disclose plural interrupt inputs it is unclear how the system disclosed in the Suh patent would have been modified into the Giles patent or the motivation for such a combination. Although the Office Action asserts that the motivation for such a combination would to be to increase the system performance by increasing the capacity and resources for processing the interrupts, the Giles patent relates to the purpose of holding or delaying an interrupt signal to ensure that it will be asserted. This appears to be contrary to the alleged motivation to combine the teachings of the two patents.

Applicants assert that one of ordinary skill in the art would not have been motivated by the disclosure of, or any suggestion in, either the Suh patent or the Giles patent to combine the teachings thereof.

As for the Monahan patent cited in the rejection of claims 5, 11 and 17, it does not, either individually or in combination, overcome the above deficiencies of the Giles and Suh patents.

Applicants' assert that the applied prior art does not disclose or suggest all of the features of the independent claims 1, 7 and 14. Therefore, claims 1-20 should be allowed.

New claim 21 further recites the feature of selectively enabling and disabling interrupt requests from each of the plurality of interrupt sources to one or more of the plurality of interrupt inputs, wherein the same interrupt source is enabled for one of the plurality of interrupt inputs and is disabled for another one of the plurality of interrupt inputs. New claim 23 recites corresponding structure.

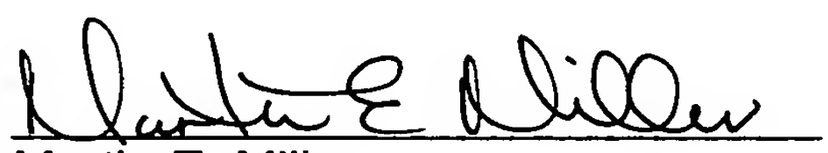
The amendment to claim 14 was made to ensure that "each interrupt input" was interpreted as referred to the "plurality of interrupt inputs" recited in the preamble. Therefore, this amendment was not made for purposes of patentability and does not narrow the scope of claim 14.

Applicants respectfully assert the features recited in the new claims are not disclosed or suggested in the prior art of record and these claims should also be indicated allowable.

Should any questions arise in connection with this application, or should the Examiner believe a telephone conference would be helpful in resolving any remaining issues pertaining to this application, the undersigned respectfully requests that he be contacted at the number indicated below.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date: August 21, 2006 By: 

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